

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 54 (canceled)

55. (currently amended) A chip package, comprising:

a semiconductor device;

a substrate comprising a solder mask and a first pad separate from with a sidewall not covered by a said solder mask, wherein said first pad is at a horizontal level same as said solder mask is at, and wherein said first pad has a circular shape;

a metal pillar between said semiconductor device and said first pad, substrate, wherein said metal pillar has a thickness ~~of~~ between 10 and 100 micrometers; microns;

~~a~~ an under bump metal layer between said metal pillar and said first pad, substrate, wherein said metal pillar has a transverse dimension smaller than that of said under bump metal layer, wherein said metal pillar has a first sidewall recessed from a second sidewall of said under bump metal layer, wherein a distance between said first sidewall and said second sidewall is greater than 0.2 micrometers, and wherein said under bump metal layer comprises ~~has a bottom~~

~~surface having a first portion region covered by over said metal pillar and a second portion region overhanging not covered by said metal pillar; and~~

~~a solder metal between said under bump metal layer and said first pad, substrate, wherein said solder metal is bonded to said first pad; and -~~

~~an underfill between said semiconductor device and said substrate, wherein said underfill contacts with said semiconductor device and said substrate and encloses said metal pillar and said solder metal.~~

Claim 56 (canceled)

57. (currently amended) The chip package of Claim 55, wherein said substrate further comprises multiple second pads at said horizontal level, wherein each of said multiple second pads has said circle shape, wherein said solder mask is separate from said multiple second pads, and wherein said first pad and said multiple second pads are aligned in a direction parallel with a sidewall of said solder mask. ~~, wherein the distance between a sidewall of said metal layer and a sidewall of said metal pillar is greater than 0.2 microns.~~

58. (currently amended) The chip package of Claim 55, wherein said semiconductor device comprises a second pad and a passivation layer, wherein said second pad is exposed by an opening in said passivation layer, and wherein said metal pillar is between said second pad and said first pad. ~~substrate.~~

59. (previously presented) The chip package of Claim 58 further comprising a barrier layer between said metal pillar and said second pad.

60. (previously presented) The chip package of Claim 55, wherein said substrate comprises a ball grid array substrate.

61. (previously presented) The chip package of Claim 55 further comprising a contact ball under said substrate, wherein said semiconductor device is over said substrate.

62. (currently amended) The chip package of Claim 55, wherein said substrate comprises multiple second pads at said horizontal level, wherein each of said multiple second pads has said circular shape, wherein said solder mask is separate from said multiple second pads, and wherein said first pad and said multiple second pads are aligned in a direction parallel with an edge of said substrate. ~~further comprising an underfill between said semiconductor device and said substrate.~~

63. (currently amended) The chip package of Claim 55, wherein said substrate comprises multiple second pads at said horizontal level, wherein each of said multiple second pads has said circular shape, wherein said solder mask is separate from said multiple second pads, and wherein said first pad and said

multiple second pads are aligned in a line. ~~further comprising a molding compound between said semiconductor device and said substrate.~~

64. (previously presented) The chip package of Claim 55, wherein said substrate further comprises a second pad at said horizontal level, wherein said second pad is separate from said solder mask, wherein said second pad is the pad closest to said first pad and has said circular shape, ~~neighboring to said first pad and having an edge not covered by a solder mask,~~ and wherein no solder mask traverses between said first and second pads

65. (currently amended) The chip package of Claim 55, wherein said substrate further comprises a second pad at said horizontal level, wherein said second pad is separate from said solder mask, wherein said second pad is the pad closest to said first pad and has said circular shape, and wherein said first pad has a diameter greater than the minimum distance between said first and second pads.
~~first region is substantially coplanar with said second region.~~